Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An interleaver memory access apparatus of a CDMA system comprising:

an interleaver memory for storing code symbols to be transmitted;

a shift register unit for simultaneously receiving 18 bit code symbols from the interleaver memory and outputting ~~it by~~the 18 bit code symbols in three sets of 6 bit code symbols;

an index decoding unit for decoding the 6 bit code symbols outputted from the shift register unit and ~~generates~~ generating a Walsh bit index;

an address generator and control logic for controlling ~~the~~ an access operation of the interleaver memory and ~~the~~ an input and output operation of the shift register unit and the index coding unit; and

an orthogonal modulator for outputting 64 bit Walsh codes ~~on the basis of~~based on the Walsh bit index outputted from the index decoding unit.

2. (Currently Amended) The apparatus of claim 1, wherein the interleaver memory simultaneously outputs ~~the 1 row~~a row of code symbols according to a row address outputted from the address generator and control logic.

3. (Original) The apparatus of claim 1, wherein the shift register unit includes two shift registers connected in series so that when one shift register performs a reading operation, the other shift register can perform a writing operation.

4. (Currently Amended) The apparatus of claim 3, wherein each shift register includes ~~3~~ three storing regions.

5. (Currently Amended) The apparatus of claim 4, wherein ~~the~~ each shift register simultaneously outputs 6 bit code symbols stored in each storing region according to a data select signal outputted from the address generator and control logic.

6. (Currently Amended) The apparatus of claim 1, wherein the index decoding unit includes ~~a~~ first, ~~through a~~second and third index decoders for sequentially receiving 6 bit code symbols ~~by 6 ones~~ from the shift register unit and generating ~~one~~ a corresponding Walsh bit index, respectively.

7. (Currently Amended) The apparatus of claim 6, wherein the first, ~~through~~ ~~the~~second and third index decoders are sequentially activated according to an enable signal outputted from the address generator and control logic.

8. (Currently Amended) The apparatus of claim 1, wherein the address generator and control logic repeatedly accesses ~~to~~ the shift register if code symbols to be transmitted are not in a full rate.

9. (Currently Amended) The apparatus of claim 8, wherein the address generator and control logic accesses the shift register ~~by~~ one time ~~in case of the~~ for a half rate, repeatedly accesses ~~to~~ the shift register ~~by~~ three times ~~in case of~~ for a quarter rate, and repeatedly accesses ~~to~~ the shift register ~~by~~ seven times ~~in case of~~ for an ~~eight~~ eighth rate.

10. (Currently Amended) An interleaver memory access method of a CDMA system comprising ~~the steps of~~:

storing code symbols to be transmitted in ~~the~~ an interleaver memory;

reading ~~1 row~~ a row of code symbols stored in the interleaver memory ~~by~~ using a row address signal and outputting ~~them~~ the row of code symbols to ~~the~~ a shift register unit;

repeatedly accessing the ~~first~~ code symbols stored in the shift register unit according to ~~the~~ a transfer rate of the code symbols; and

decoding the ~~6~~ code symbols outputted from the shift register unit and generating one Walsh index.

11. (Currently Amended) The method of claim 10, wherein the interleaver memory writes symbol codes according to ~~a~~ row and ~~a~~ column addresses and reads symbol codes according to a row address.

12. (Original) The method of claim 10, wherein the shift register unit includes two shift registers connected in series so that when one shift register performs a reading operation, the other shift register can perform a writing operation.

13. (Currently Amended) The apparatus of claim 10, wherein each shift register includes ~~3~~ three storing regions, and each region stores ~~6~~ six code symbols.

14. (Original) The apparatus of claim 10, wherein if the transfer rate of the code symbols is the full rate, the shift register is not repeatedly accessed.

15. (Currently Amended) The apparatus of claim 10, wherein the shift register is accessed ~~by one time~~ once if the transfer rate is a half rate, repeatedly accessed ~~by~~ three times ~~in case of~~ for a quarter rate, and repeatedly accessed ~~by~~ seven times ~~in case of~~ for an ~~eight~~ eighth rate.

16. (New) A method of accessing an interleaver in a mobile communication system, comprising:

receiving only a row address from an address generator; and

reading code symbols stored in a row of the interleaver memory corresponding to the received row address.

17. (New) The method of claim 16, further comprising:

outputting the read code symbols to a shift register unit.

18. (New) The method of claim 16, wherein the row address includes each row in the interleaver memory for a full data rate.

19. (New) The method of claim 16, wherein the row address include consecutive odd row numbers in the interleaver memory for a half data rate.

20. (New) The method of claim 19, further comprising:

outputting the read code symbols corresponding to the consecutive odd row members in the interleaver memory to a shift register unit; and

using the code symbols from a previous odd row number as code symbols corresponding to an even row number so a data size of the code symbols are the same as that for a full rate.